

4 to a subscriber through a tip terminal and a ring terminal;

5 a second [pair of transistors (Q3, Q4)] third transistor and a fourth transistor having a
6 Darlington structure, [and] connected to said first and second transistors [(Q1, Q2)] respectively, and
7 limiting a maximum current;

8 a first pair of current supervising resistors [(R1, R2)] respectively connected to emitters of
9 said first [pair of] and second transistors [(Q1, Q2) respectively] for, performing a current feedback
10 operation to limit said maximum current[,] and for detecting [in] a voltage [form] from a line current
11 flowing through telephone lines;

12 a first resistor [(R3)] connected between a collector of one of said first [pair of transistors
13 (Q1)] transistor and a collector of [one of] said [second] third transistor [(Q3)], preventing [one of]
14 said first [pair of transistors (Q1)] transistor from being saturated;

15 a second resistor [(R4)] connected between a collector of [the other one of] said second
16 [transistors (Q2)] transistor and a collector of [the other one of] said [second pair of transistors (Q4)]
17 fourth transistor, preventing said second transistor [(Q2)] from being saturated;

18 a [group] plurality of bias resistors [(R5, R6, R7)] for determining a threshold value of said
19 maximum current and [maintaining] allowing said first [pair of] and second transistors [(Q1, Q2)]
20 in an active state;

21 a [first] pair of first capacitors [(C5, C6)] superimposing a received [AC audio] signal on a
22 DC line current;

23 a pair of composite impedances [(ZL1, ZL2)] for matching a line characteristic impedance;
24 a third resistor [(R11)] for converting said line current flowing through a first one of [the]

25 said current supervising resistors [(R1)] into an input current for detecting an off-hook state;
26 an operational amplifier [(AMP3)] inversion-amplifying a signal inputted through said third
27 resistor [(R11)]; and
28 a fourth transistor [(Q6)] converting a level of a signal inversion-amplified by said
29 operational amplifier.

1 2. (Amended) The [analog subscriber matching] interface circuit of claim 1, further
2 comprising a pair of amplifiers [(AMP1, AMP2)] connected to said composite impedances [(ZL1,
3 ZL2)], respectively, for receiving and amplifying the audio signal.

1 3. (Amended) The [analog subscriber matching] interface circuit of claim 2, further
2 comprising a pair of protection elements [(CR1, CR2)] for protecting said amplifiers for amplifying
3 said audio signal from an over current through lines.

1 4. (Amended) The [analog subscriber matching] interface circuit of claim 3, further
2 comprising a dummy load resistor [(R8)] connected between the collector of [one of] said first [pair
3 of transistors (Q1)] transistor and the collector of [the other one of] said [first pair of transistors
4 (Q2)] second transistor for supplying a bias current to said first [pair of] and second transistors (Q1,
5 Q2) to prevent said first [pair of] and second transistors [(Q1, Q2)] from being saturated when no
6 load exists on said line.

1 5. (Amended) The [analog subscriber matching] interface circuit of claim 4, further
2 comprising a pair of temperature compensating diodes [(D1, D2)] connected to opposite sides of said
3 plurality of bias [resistor group (R5, R6)] registers, respectively, for preventing said first [pair of]
4 and second transistors [(Q1, Q2)] from being overheated due to a variation of the threshold value
5 of said maximum current caused by the heat generated from said first [pair of] and second transistors
6 [(Q1, Q2)] due to the line current.

1 6. (Amended) The [analog subscriber matching] interface circuit of claim 5, further
2 comprising a plurality of bypass capacitors [(C1, C2, C3)] preventing a bad influence on call
3 communications due to the generation or induction of noise in said DC line current supply.

1 7. (Amended) The [analog subscriber matching] interface circuit of claim 6, further
2 comprising a fifth resistor [(R13)] for determining an amplification factor of said signal inputted
3 through said third resistor [(R11)].

1 8. (Amended) The [analog subscriber matching] interface circuit of claim 7, further
2 comprising a sixth resistor [(R10)] for detecting a ring trip voltage if a telephone handset is hooked
3 off during supply of a call signal.

1 9. (Amended) The [analog subscriber matching] interface circuit of claim 8, further
2 comprising a seventh resistor [(R12)] converting the voltage detected by said sixth resistor [(R10)]

3 into a ring trip current.

1 10. (Amended) The [analog subscriber matching] interface circuit of claim 9, further
2 comprising a second capacitor [(C7)] allowing said operational amplifier [(AMP3)] to serve as a
3 low-pass filter so that an AC amplification factor is greatly lowered to remove AC ripple
4 components included in said ring trip current.

1 11. (Amended) The [analog subscriber matching] interface circuit of claim 10, further
2 comprising a field effect transistor [(FET1)] allowing said operational amplifier [(AMP3)] to serve
3 as a low-pass filter in a ring current supply state.

4 --12. A subscriber line interface circuit, comprising,
5 a first terminal having a first reference voltage;
6 a second terminal having a second reference voltage;
7 a first voice line; and
8 a first current limiting circuit connected between said first terminal and said first voice line,

9 including:

10 a first transistor a having an emitter, a collector connected to said first voice line,
11 and a base;
12 a first current supervising register connected between said emitter of said first
13 transistor and said first terminal;

14 a second transistor having an emitter connected to said base of said first transistor,
15 a collector, and a base;
16 a second register connected between said collectors of said first and said second
17 transistor;
18 a third register connected between said base of said second transistor and said first
19 terminal; and
20 a fourth register connected between said base of said second transistor and said
21 second terminal.

1 --13. The subscriber line interface circuit of claim 12, further comprised of:
2 a second line; and
3 a second current limiting circuit connected between said second terminal and said fourth
4 transistor, including:
5 a third transistor a having an emitter, a collector connected to a second line, and a
6 base;
7 a second current supervising register connected between said emitter of said first
8 transistor and said second terminal;
9 a fourth transistor having an emitter connected to said base of said third transistor,
10 a collector, and a base;
11 a fifth register connected between said collectors of said third and fourth transistor;
12 and

13 a sixth register connected between said base of said second transistor and said second
14 terminal.

1 --14. The subscriber line interface circuit of claim 13, further comprised of said a
2 dummy register coupled between said first line and said second line.

1 --15. The subscriber line interface circuit of claim 12, further comprised of a first
2 capacitor connected between said base of said first transistor and said first terminal.

1 --16. The subscriber line interface circuit of claim 12, further comprised of a second
2 capacitor connected between said base of said second transistor and said first terminal.

1 --17. The subscriber line interface circuit of claim 13, further comprised of a third
2 capacitor connected between said base of said third transistor and said second terminal.

1 --18. The subscriber line interface circuit of claim 13, further comprised of a fourth
2 capacitor connected between said base of said fourth transistor and said second terminal.

1 --19. The subscriber line interface circuit of claim 13, further comprised of:
2 an seventh register;
3 an operational amplifier connected to said emitter of said first transistor and said first

4 reference terminal through a eighth register; and
5 a switch connecting said seventh register to said amplifier and said eighth register during an
6 off hook state.

1 --20. The subscriber line interface circuit of claim 13, further comprised of:
2 a first pair of temperature compensating diodes connected between said first terminal and
3 said base of said second transistor; and
4 a second pair of temperature compensating diodes connected between said second terminal
5 and said base of said fourth transistor.